

Fig. 1

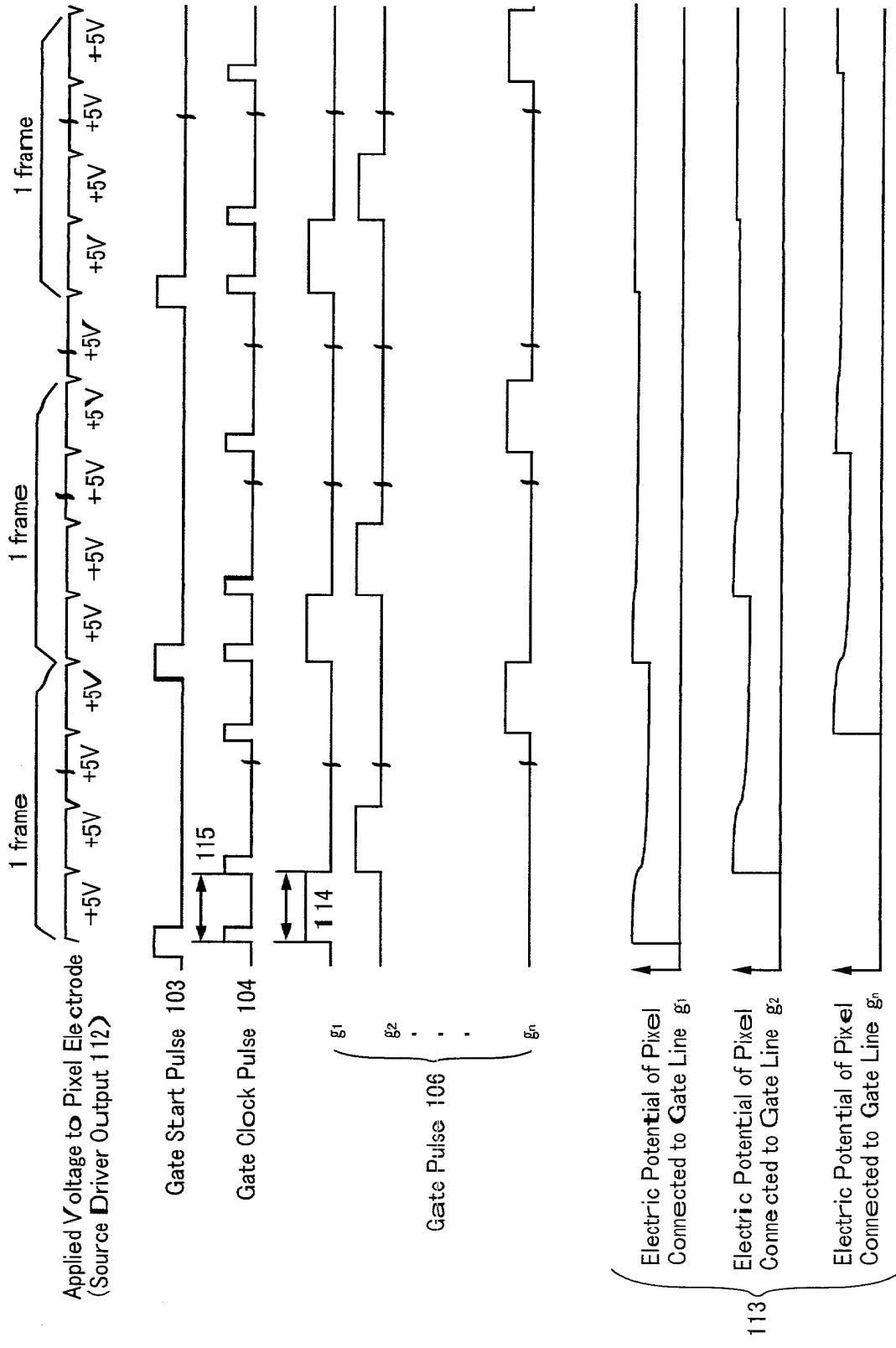


Fig. 2

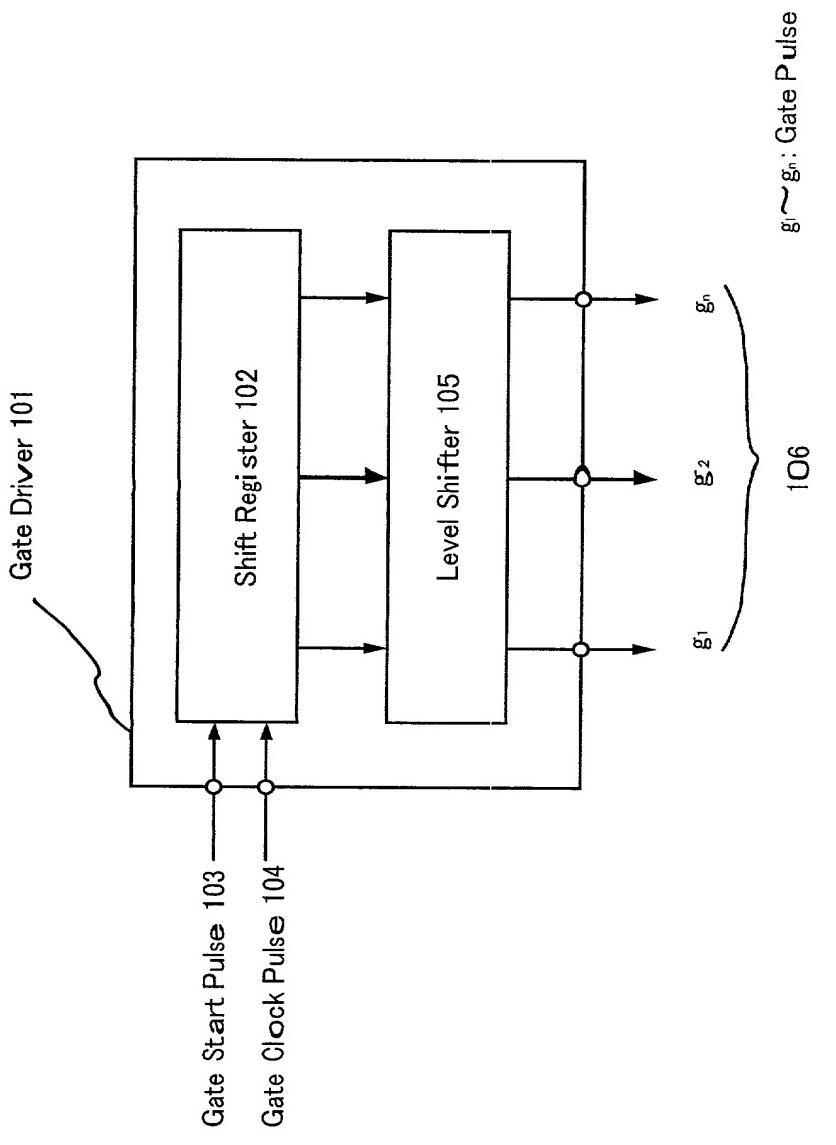


Fig. 3

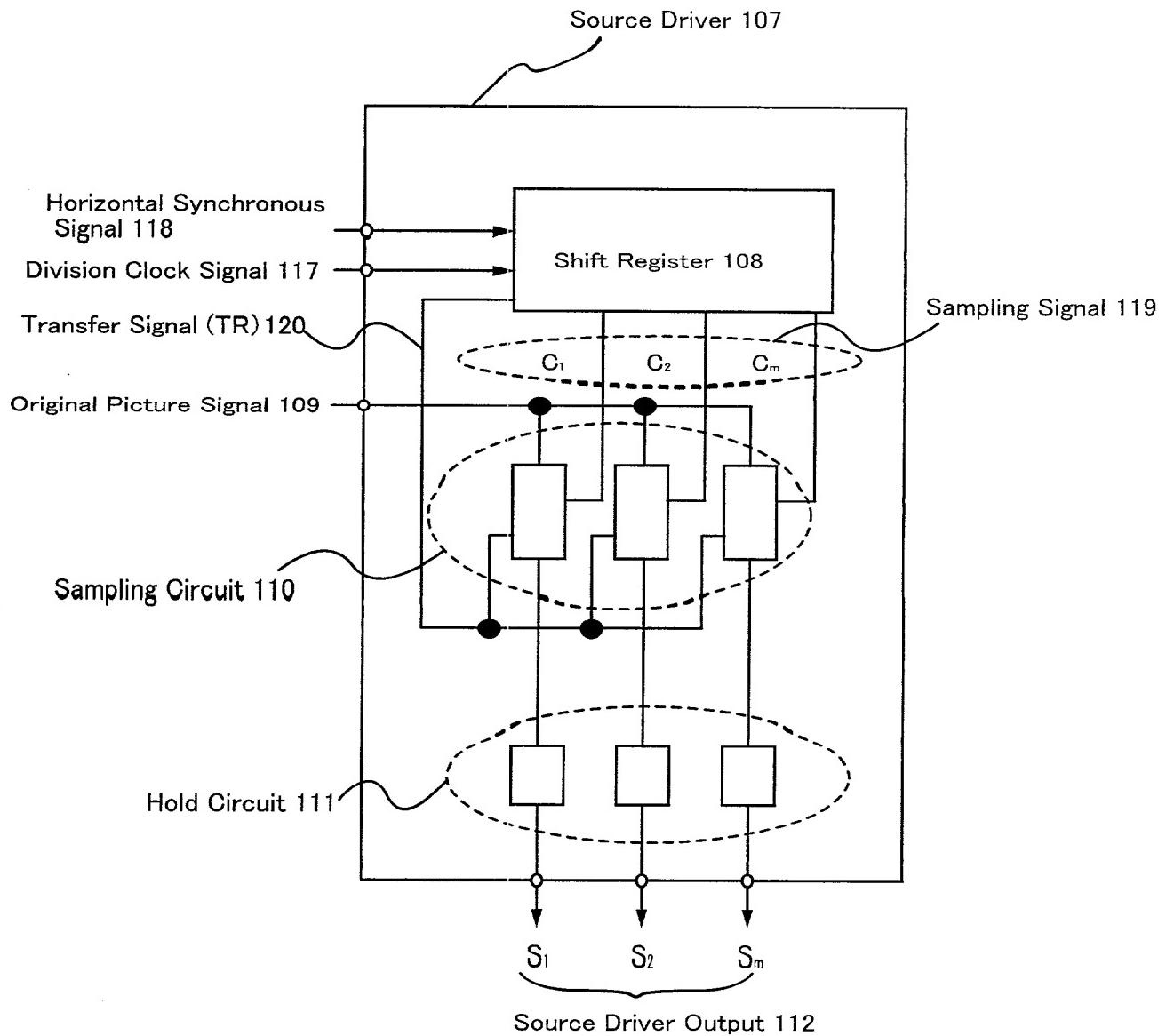


Fig. 4

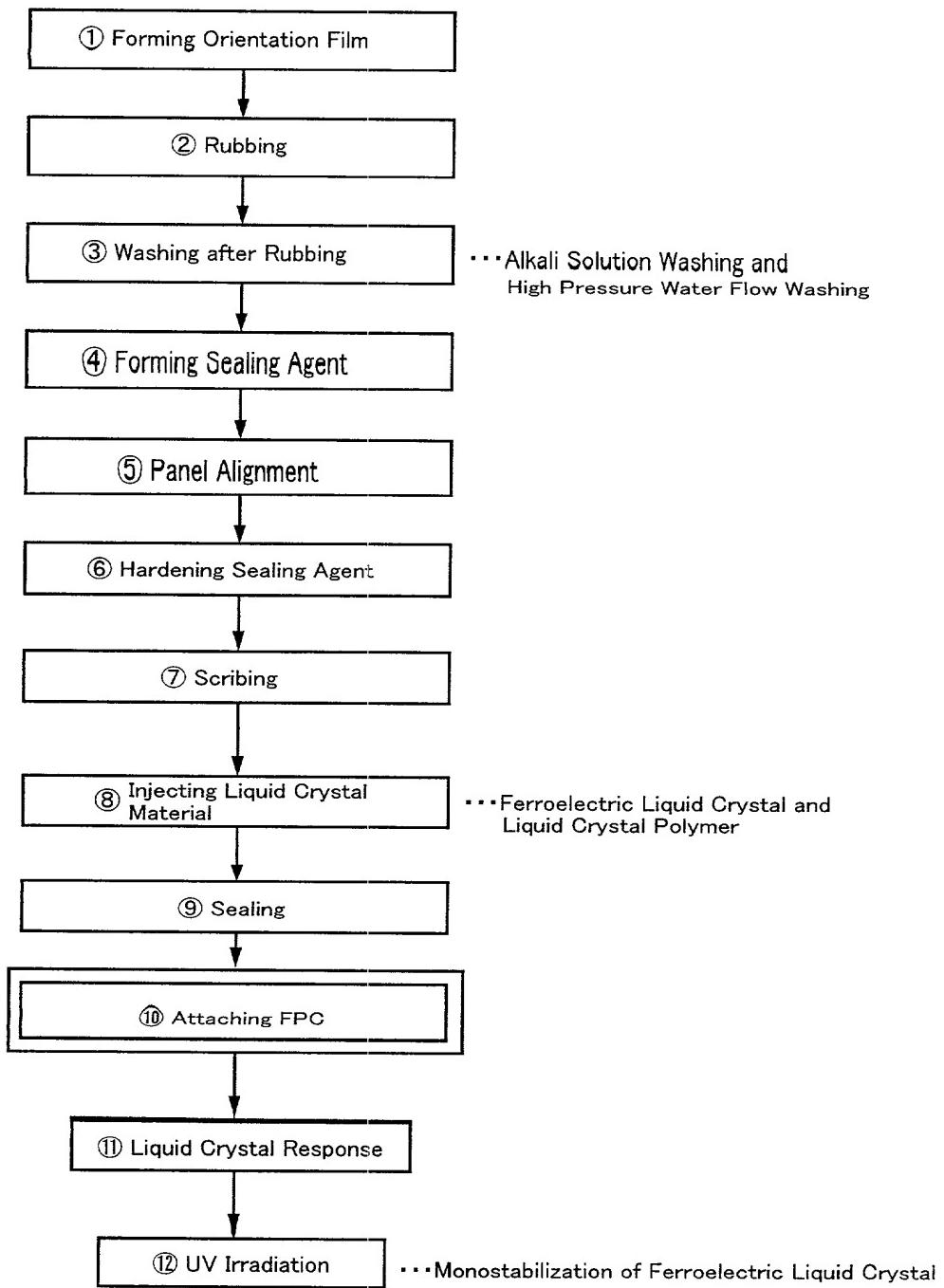


Fig. 5

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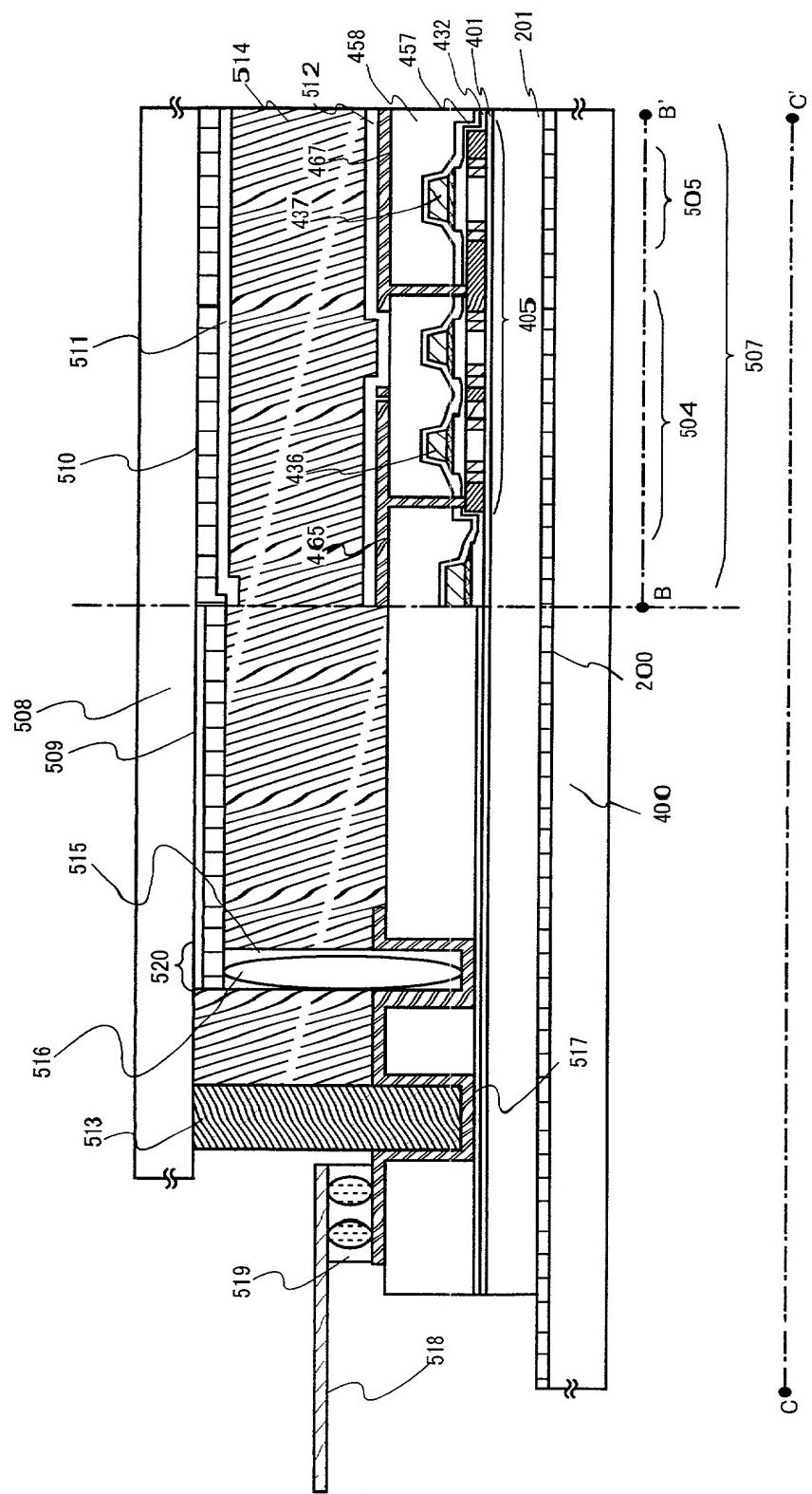


Fig. 6

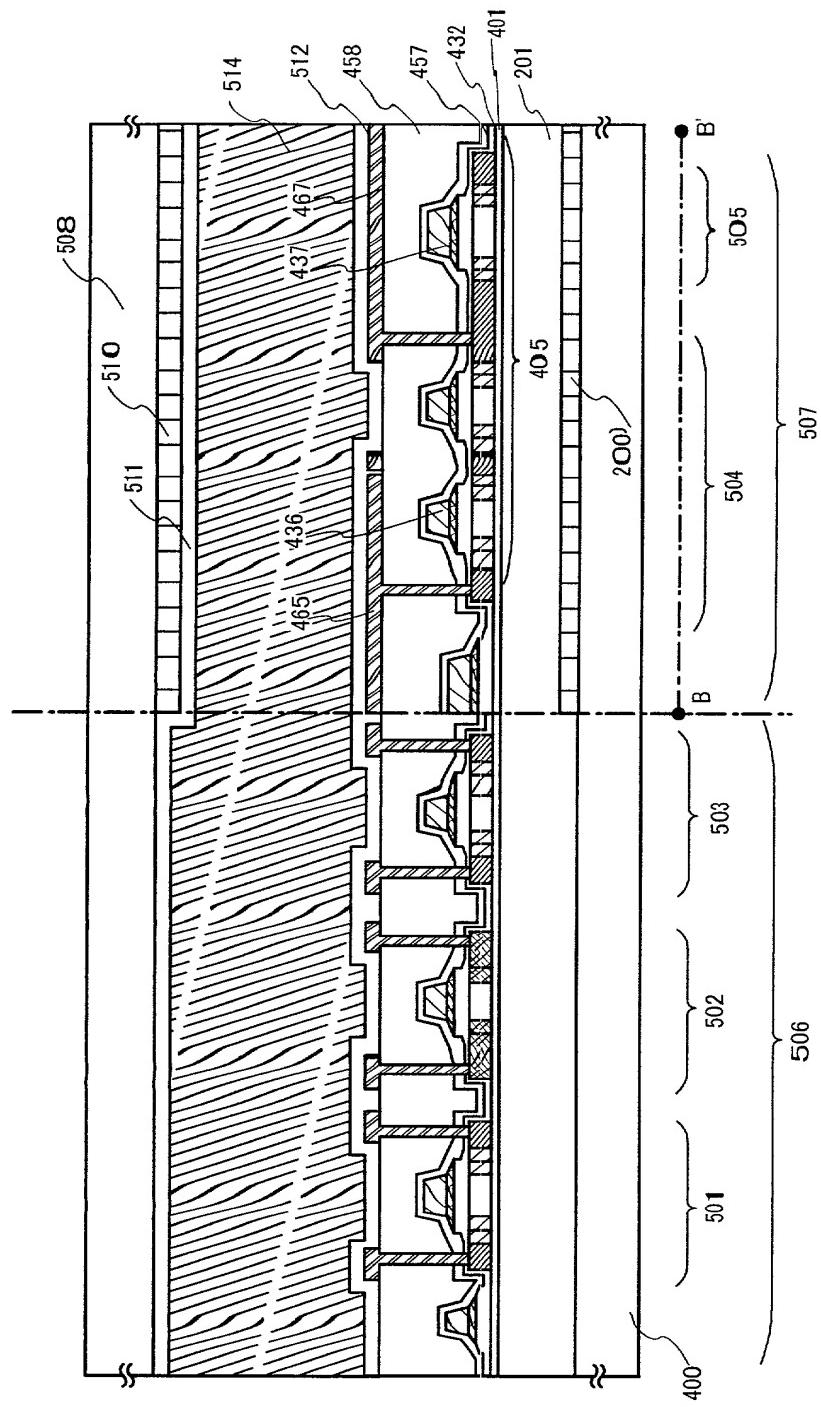


Fig. 7

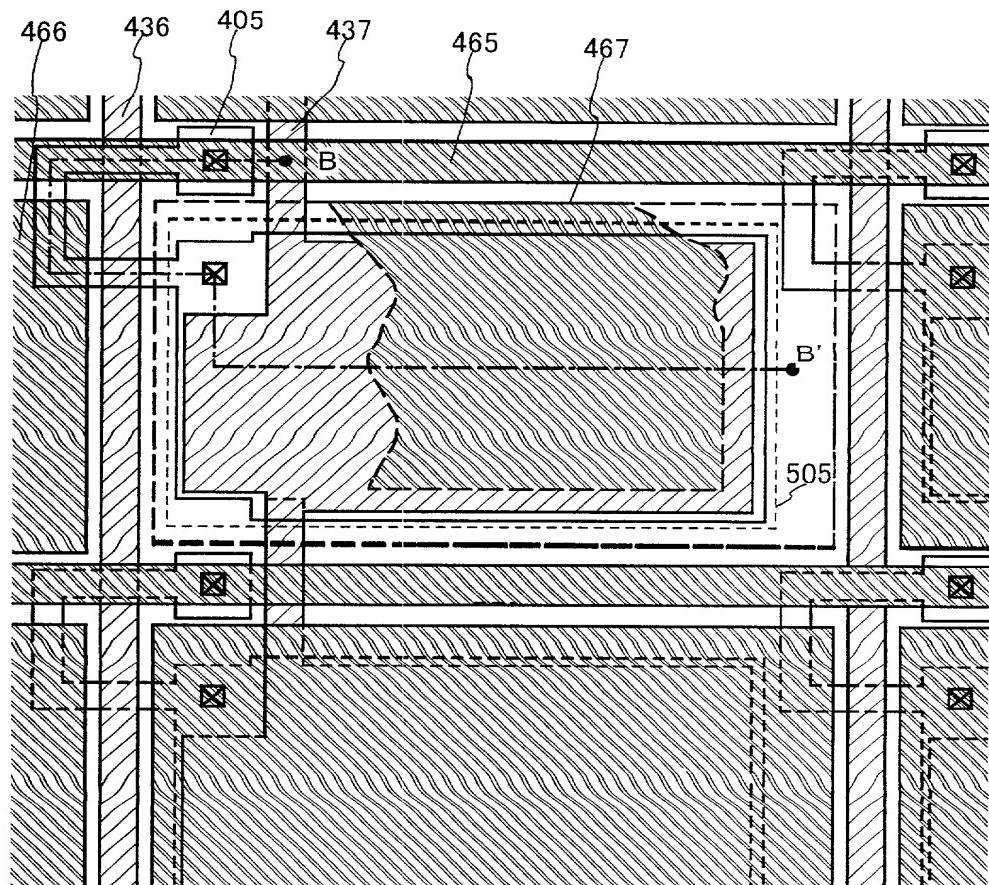


Fig. 8

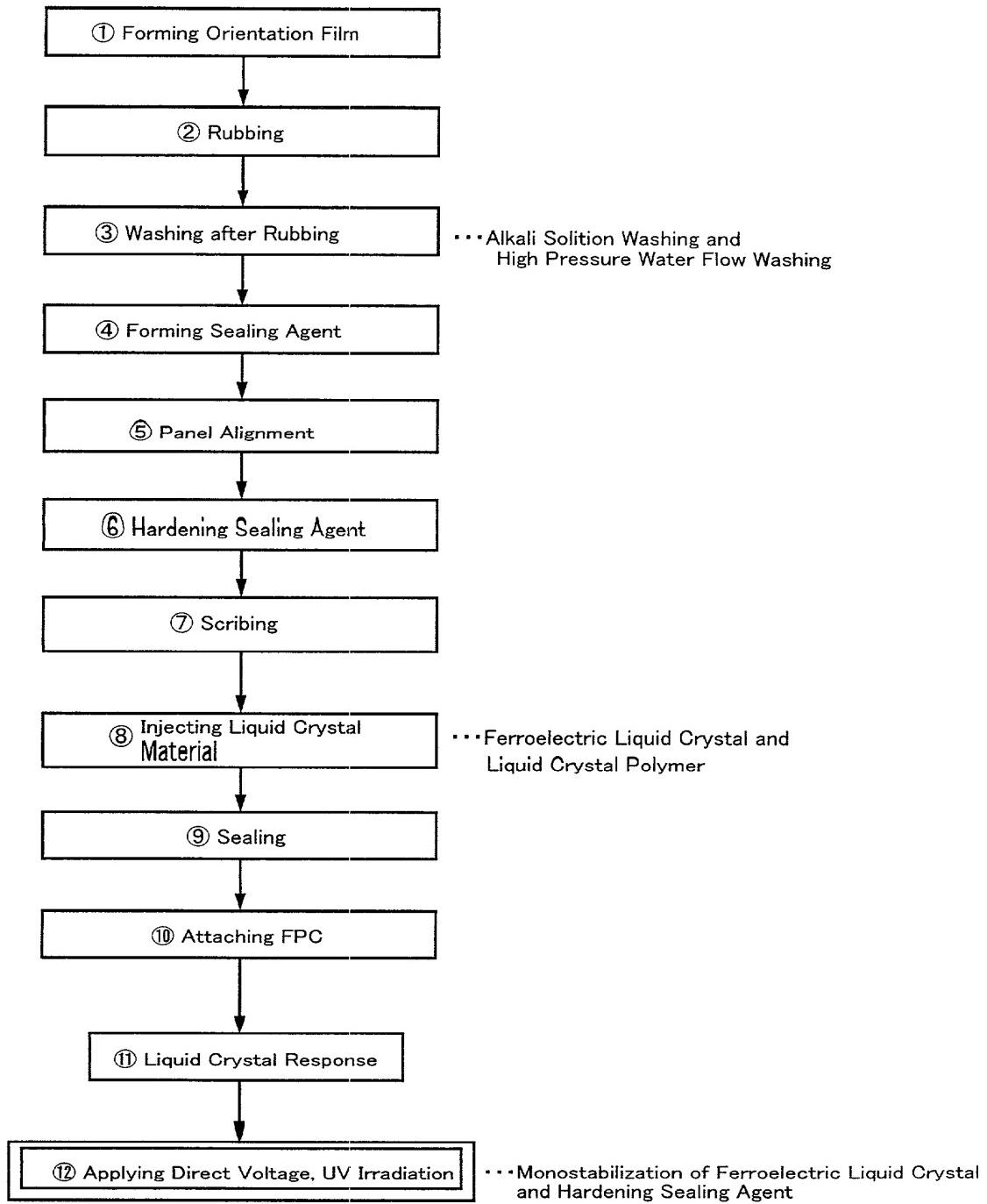


Fig. 9

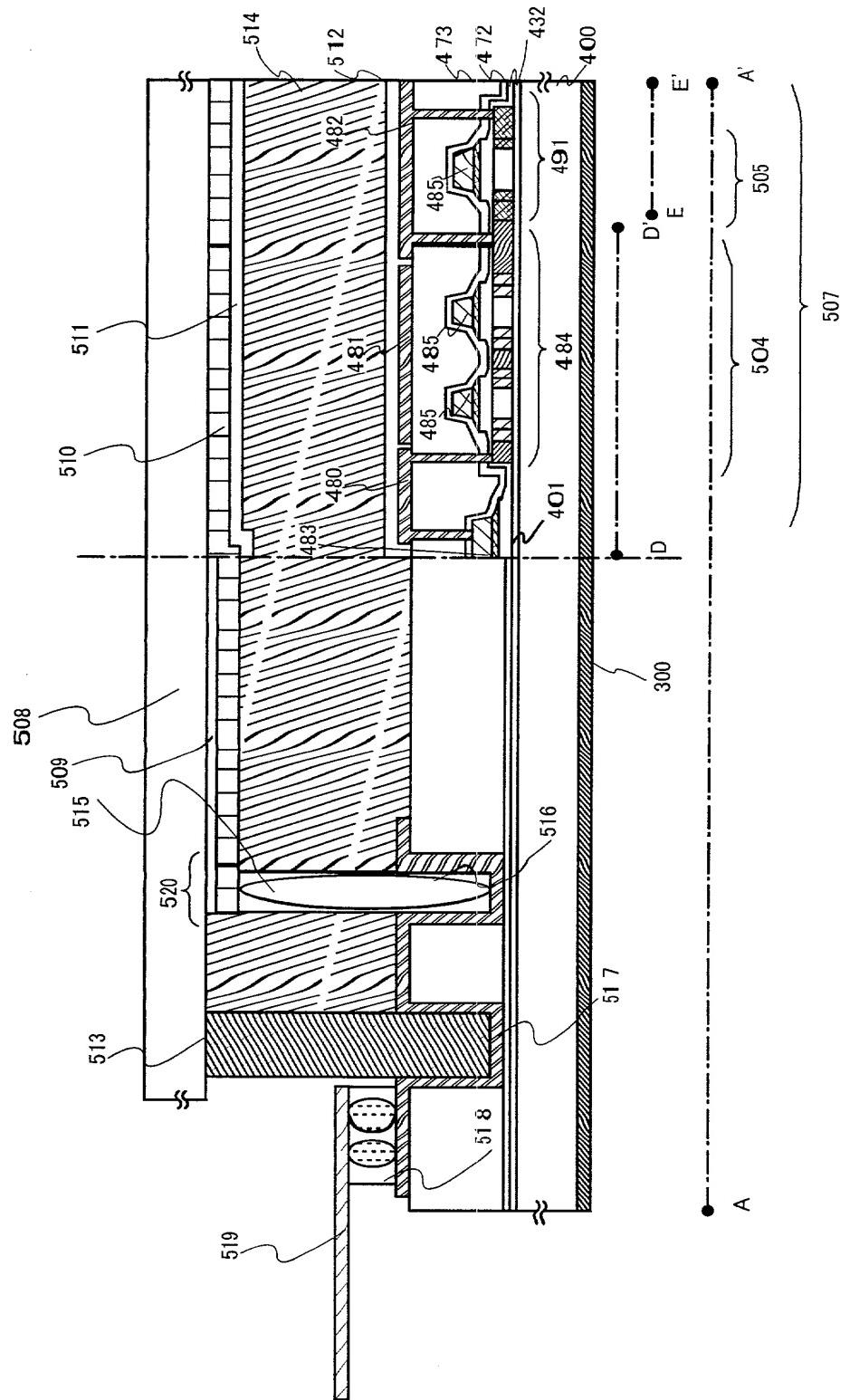


Fig. 10

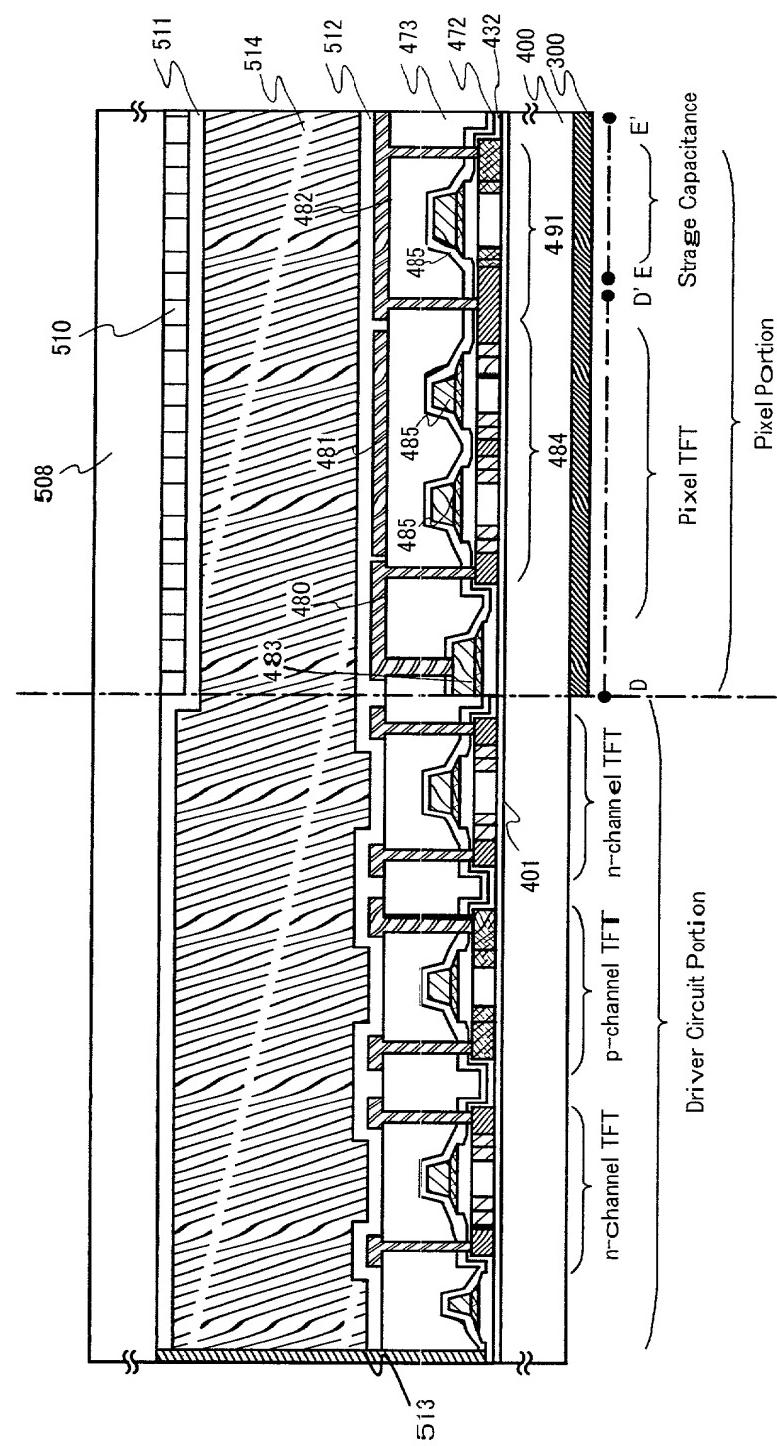


Fig. 11

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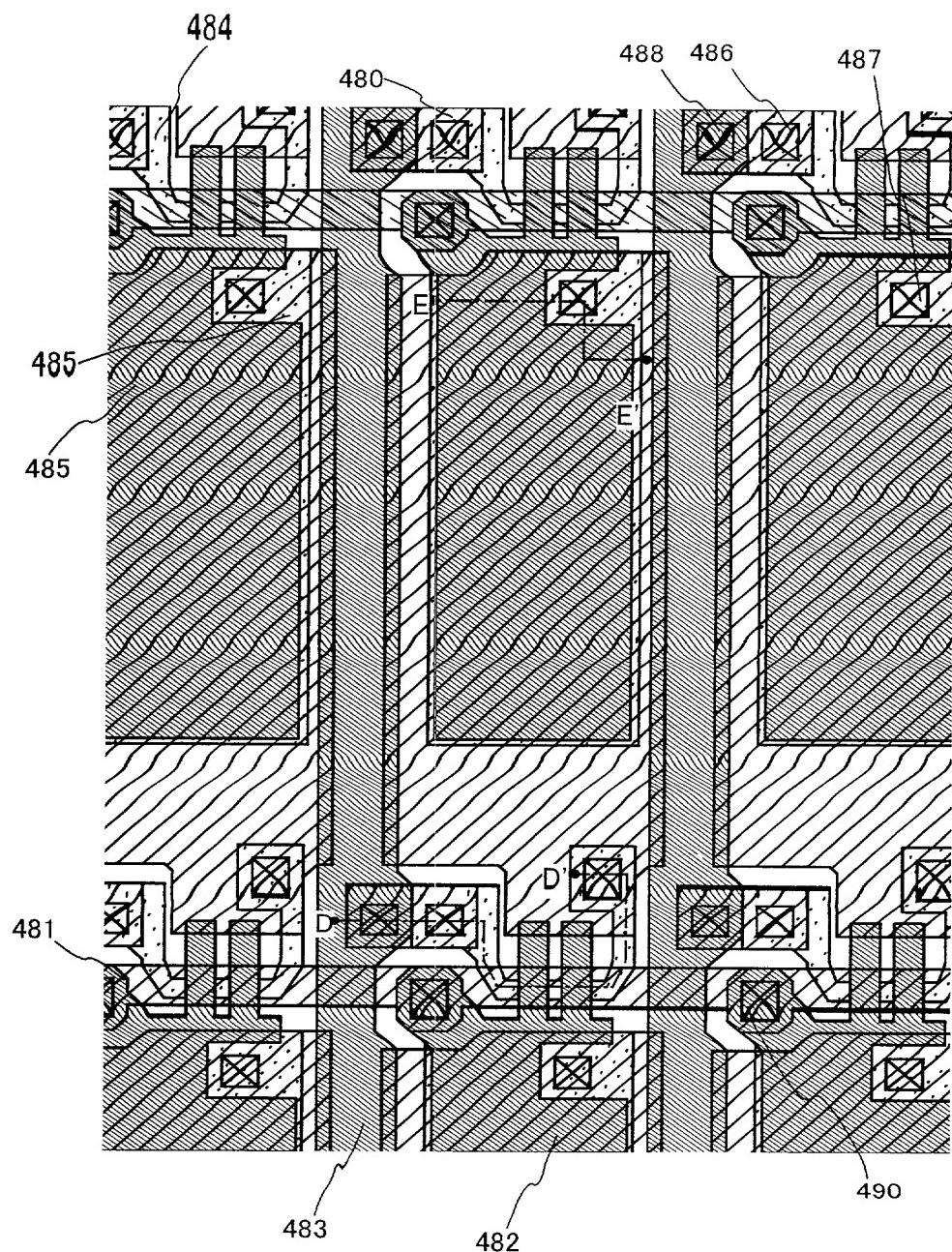


Fig. 12

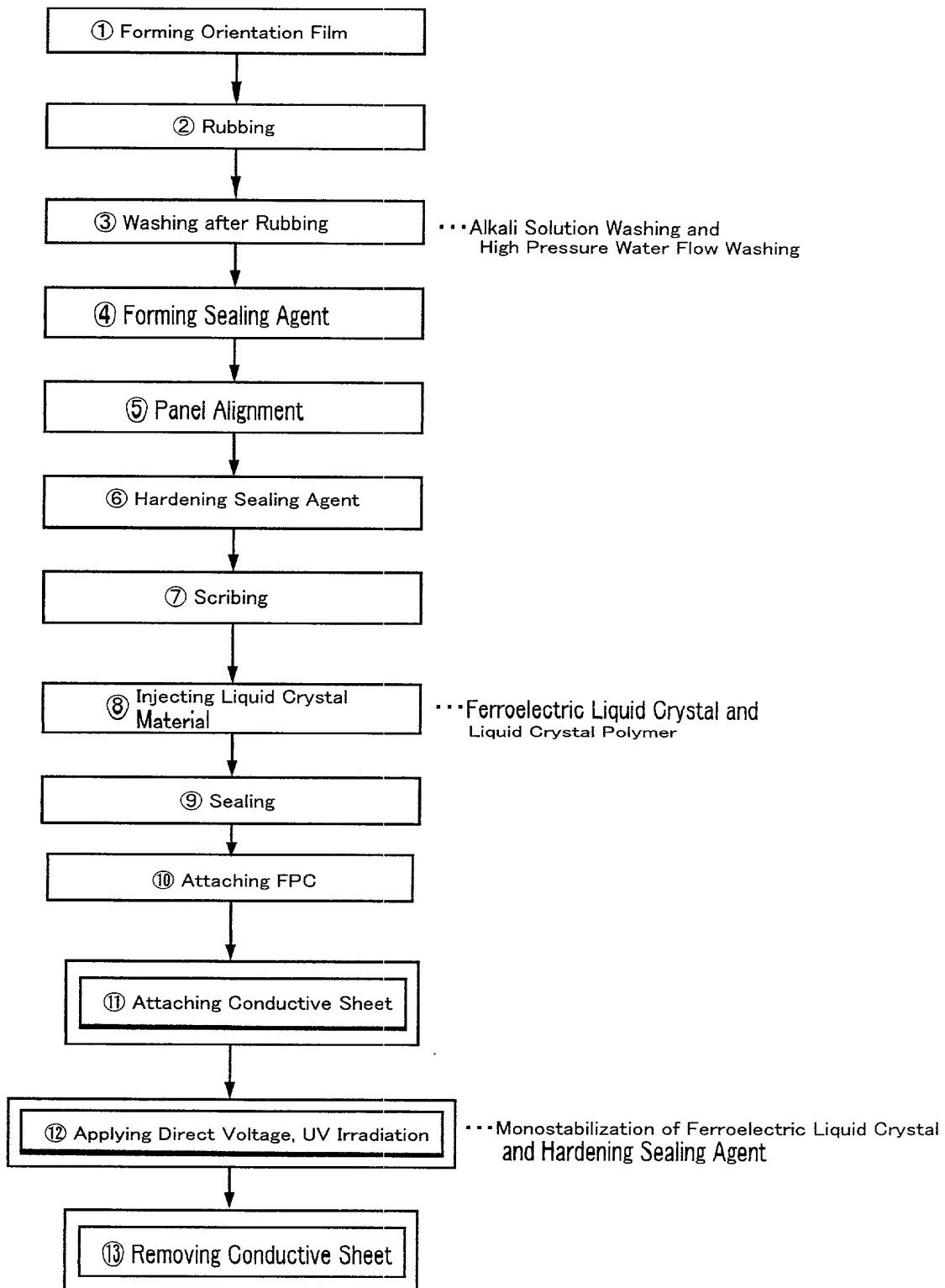


Fig. 13

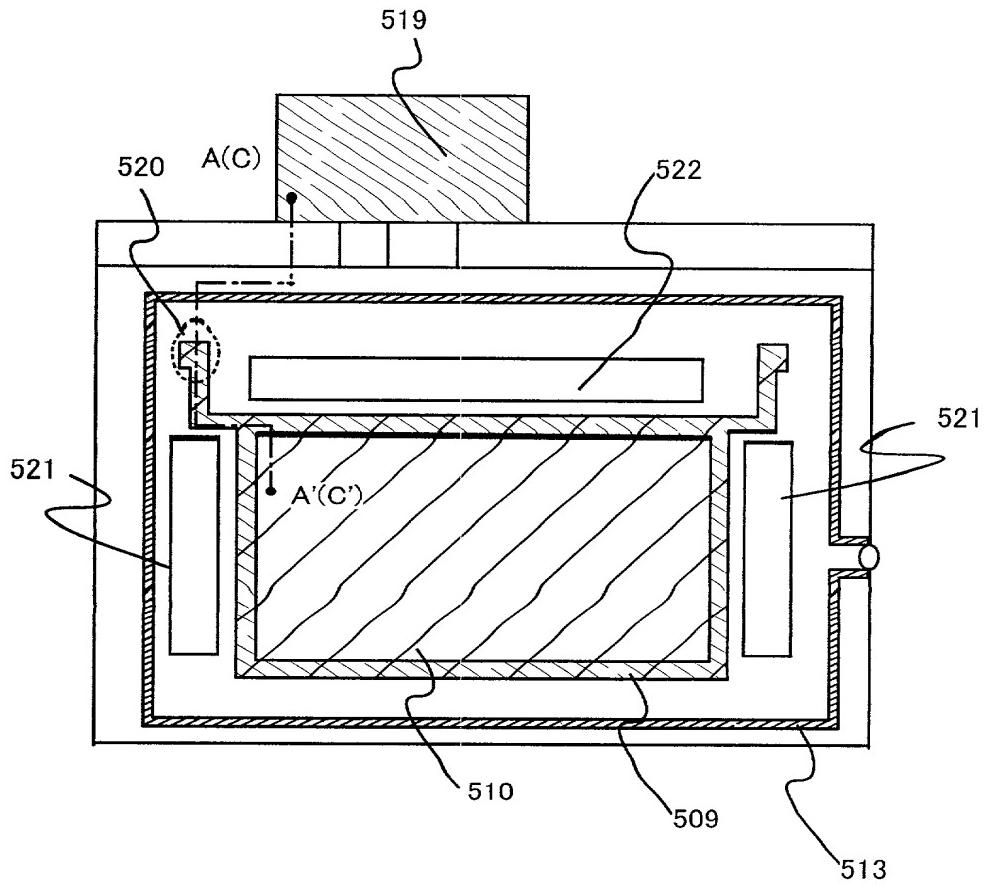
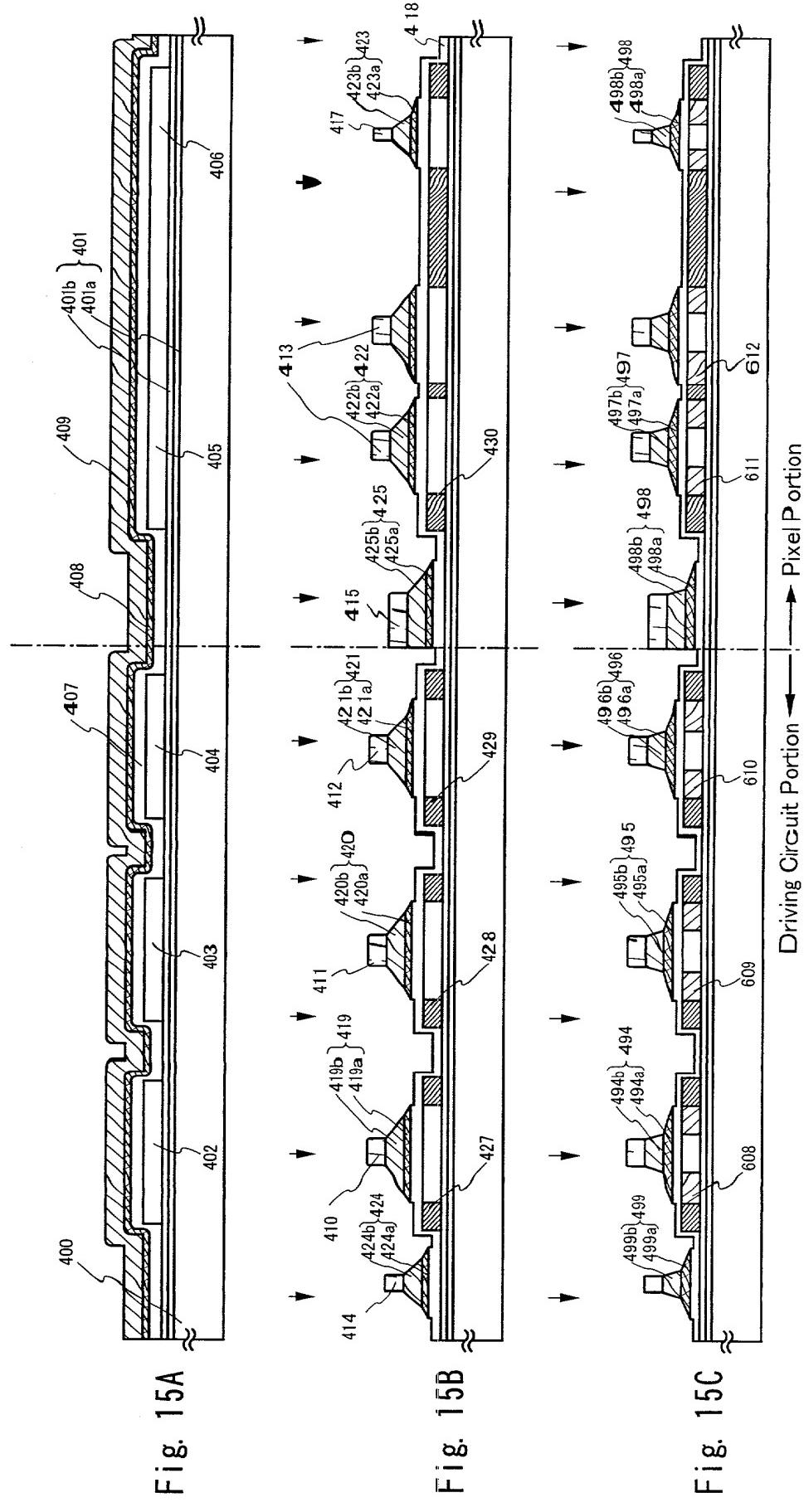


Fig. 14



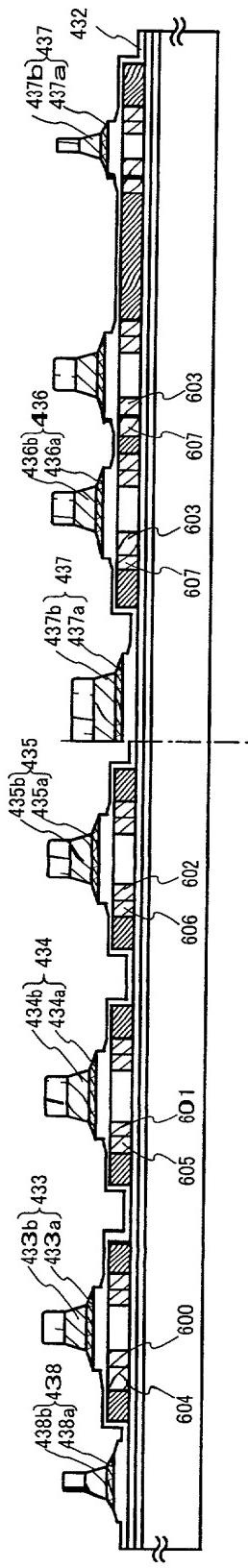


Fig. 16A

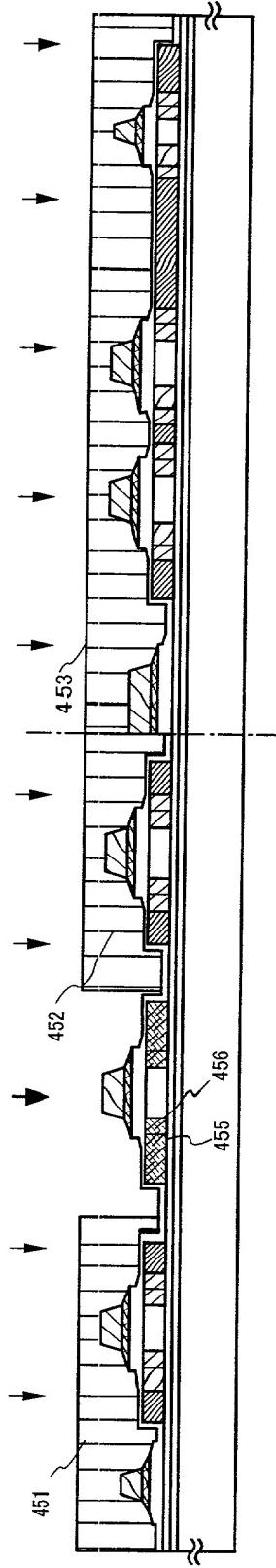


Fig. 16B

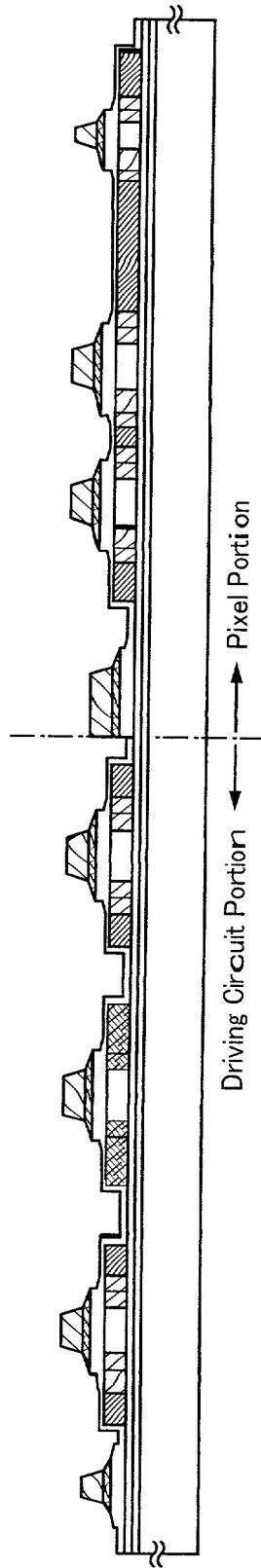


Fig. 16C

Driving Circuit Portion → Pixel Portion

Fig. 17

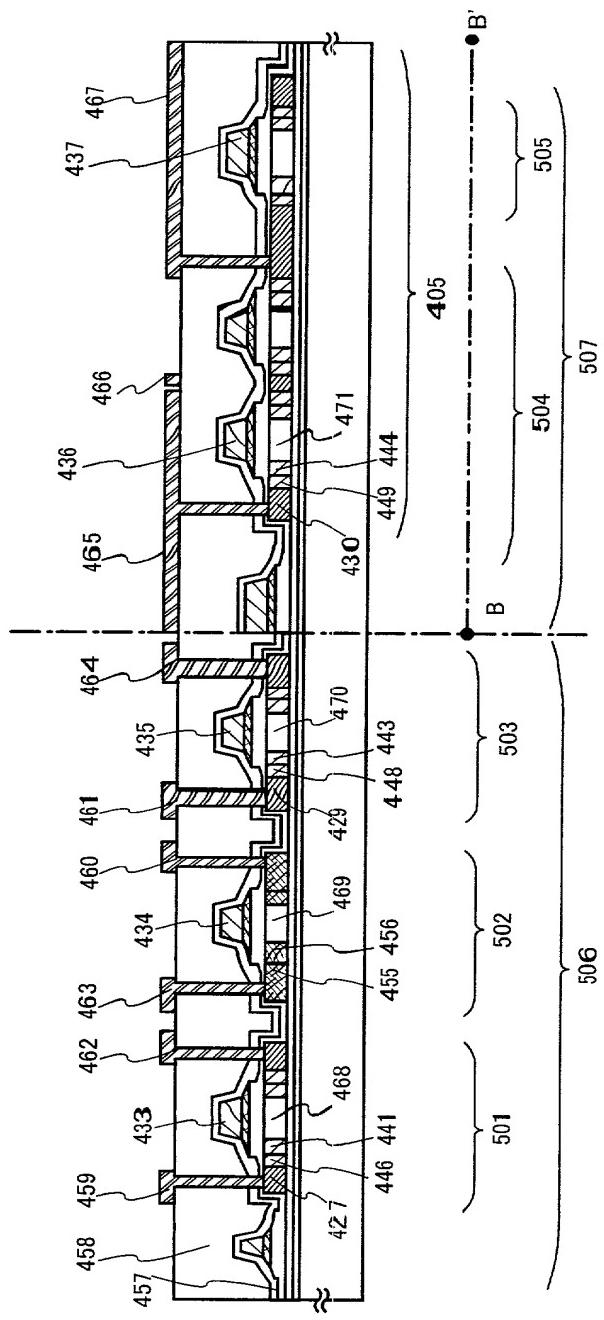
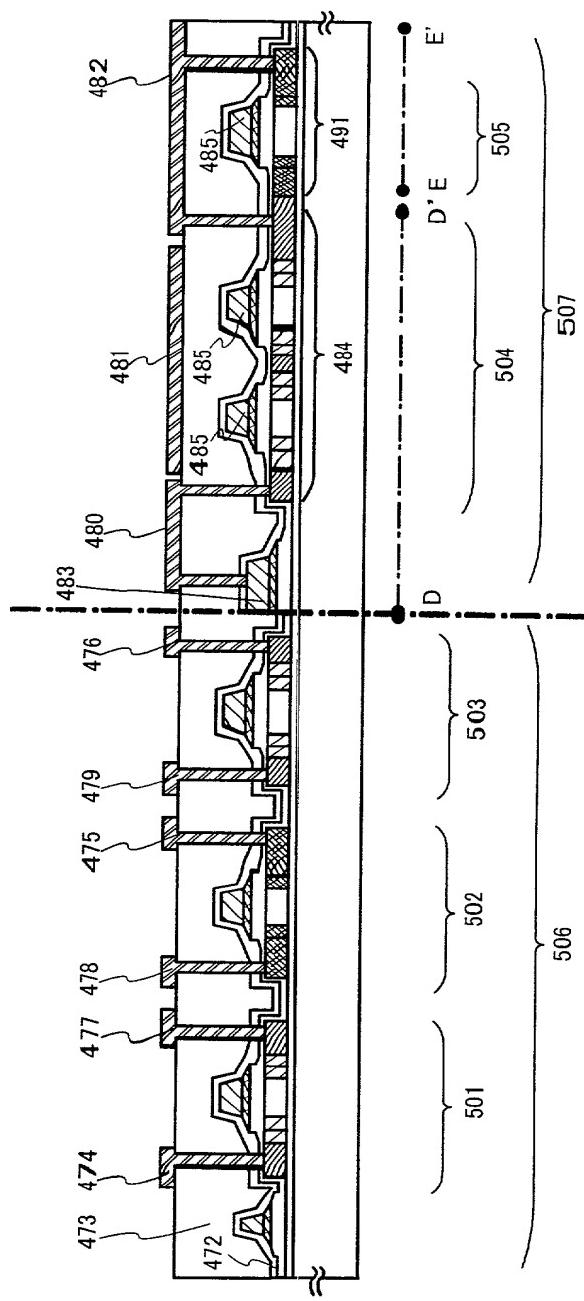


Fig. 18



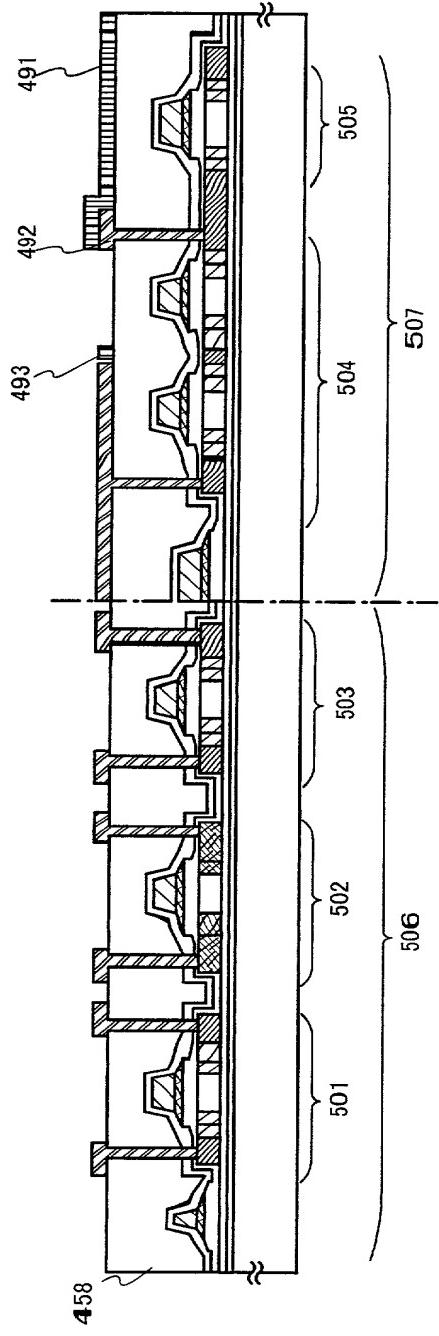


Fig. 19A

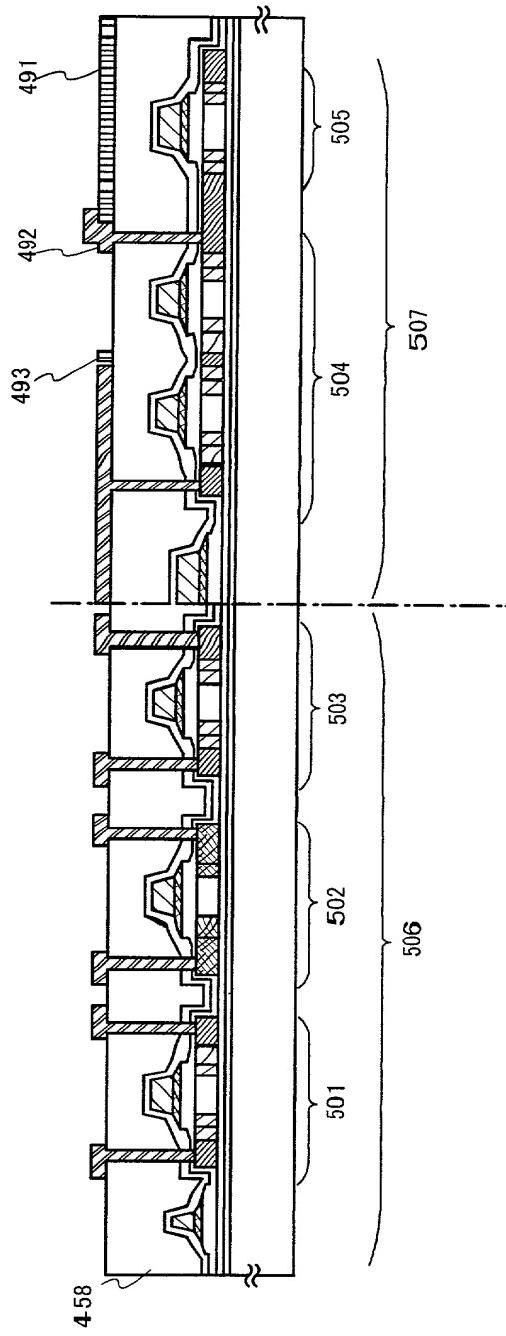


Fig. 19B

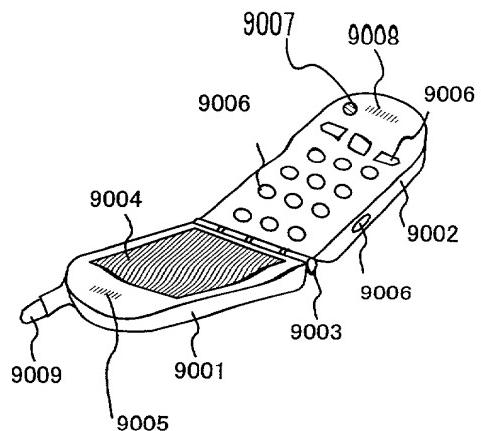


Fig. 20A

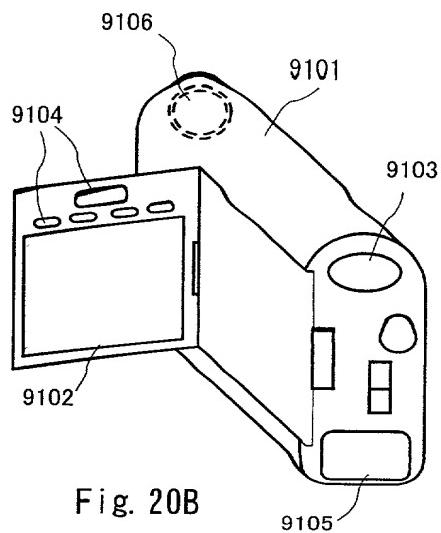


Fig. 20B

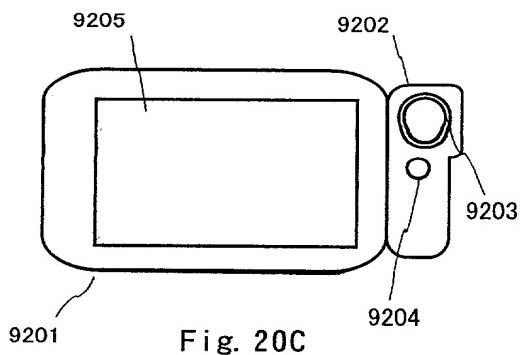


Fig. 20C

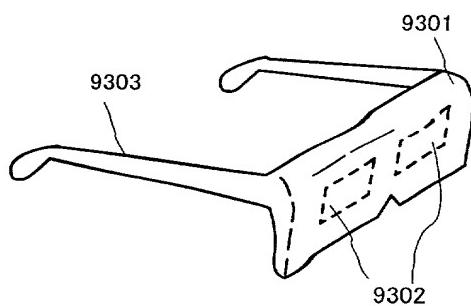


Fig. 20D

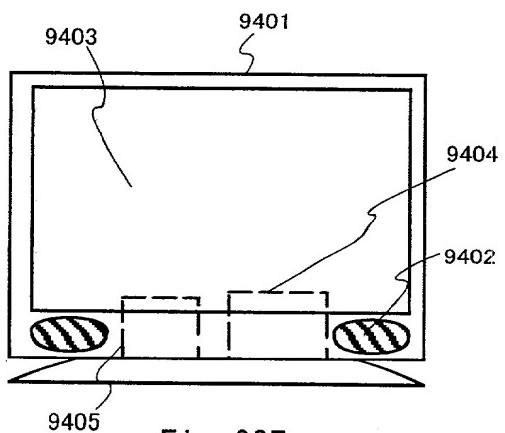


Fig. 20E

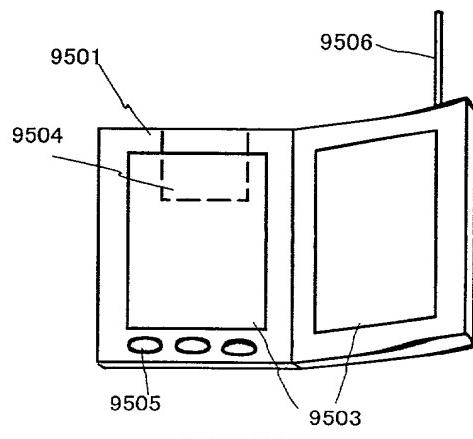
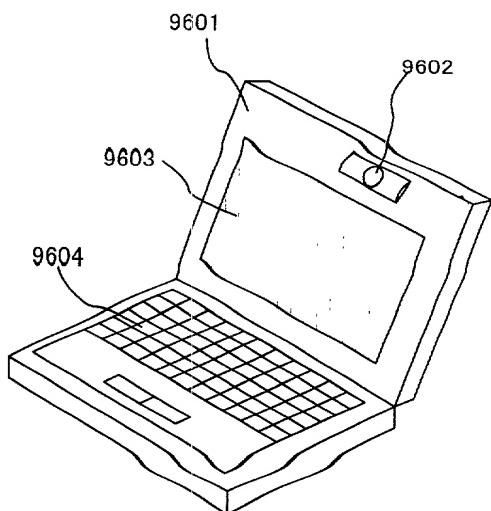
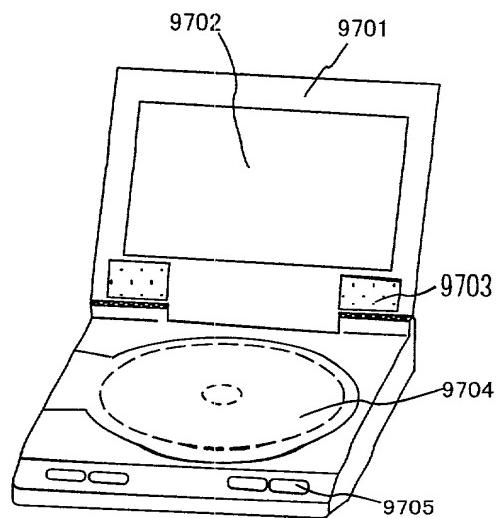


Fig. 20F

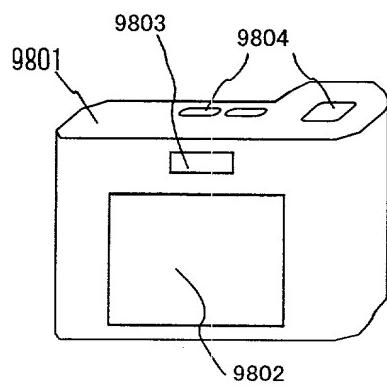
**Fig. 21A**



**Fig. 21B**



**Fig. 21C**



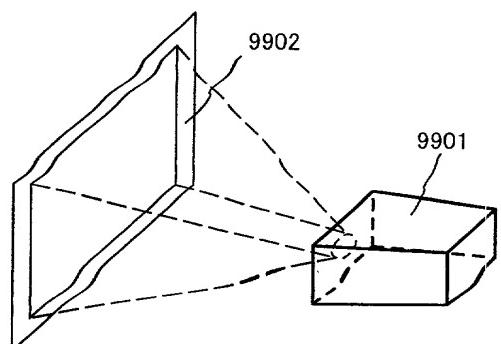


Fig. 22A

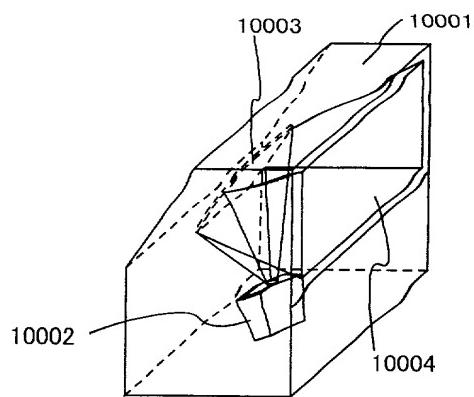


Fig. 22B

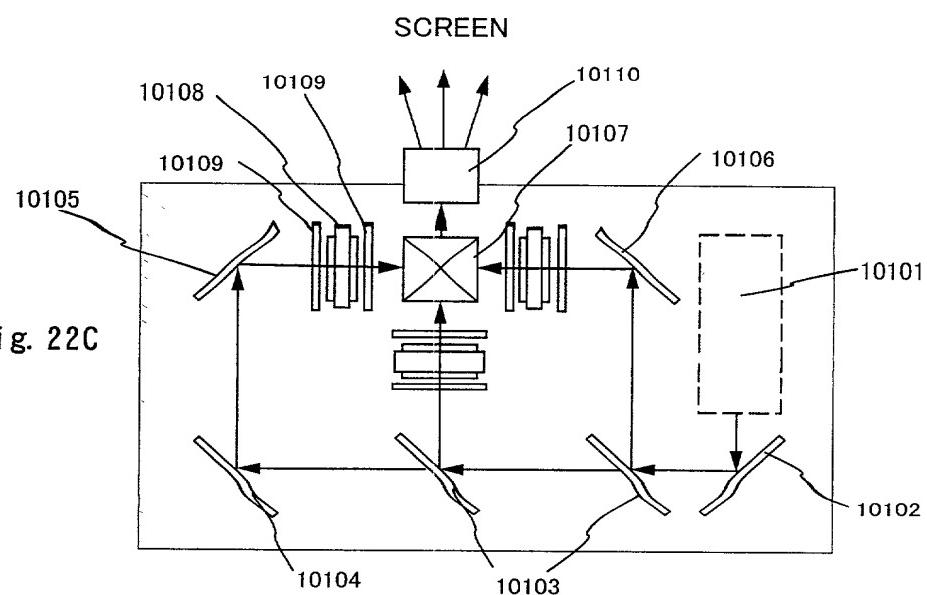


Fig. 22C

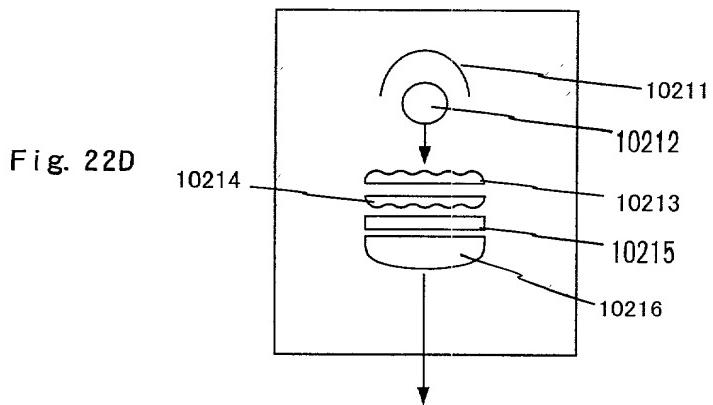


Fig. 22D

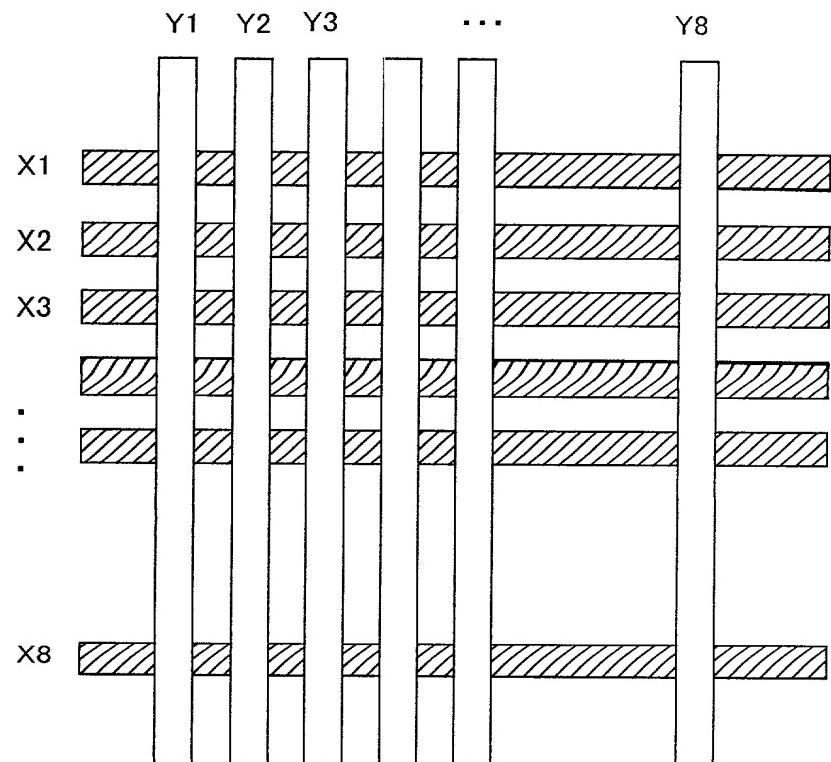


Fig. 23

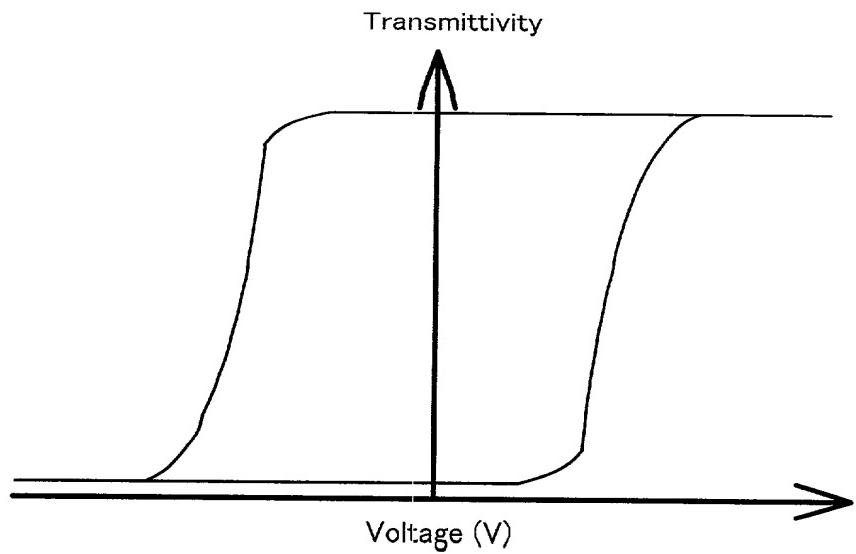


Fig. 24A

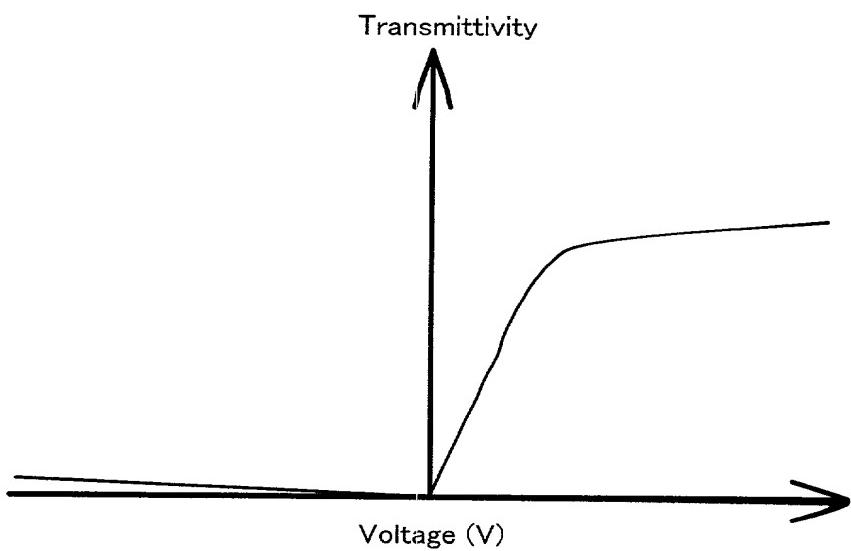


Fig. 24B

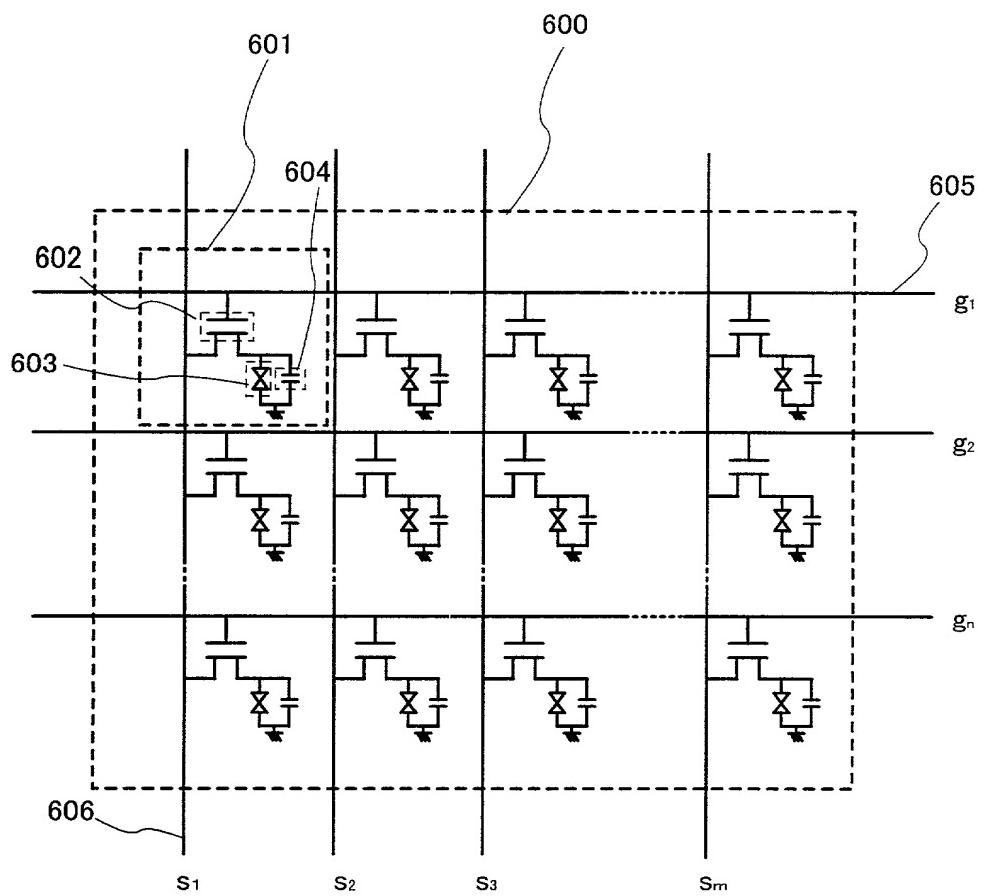


Fig. 25